ACTIVE COPLANAR UP-CONVERTER FOR HIGH GAIN V-BAND APPLICATIONS

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ABSTRACT

This paper reports on the design of a coplanar up-converter from C- to V-band on GaAs. An optimum conversion gain (62-64 GHz: G_c>4 dB) has been achieved from a non-linear optimisation, utilising a modified Tajima model for the PM-HFETs and an accurate library for the coplanar elements integrated into the CAD tool Libra. Due to the use of coplanar lumped elements, a very compact circuit size of 2.1 mm^2 has been obtained. The evaluation of the circuit demonstrates the excellent agreement of the linear and non-linear measured and simulated mixer behaviour up to 64 GHz.

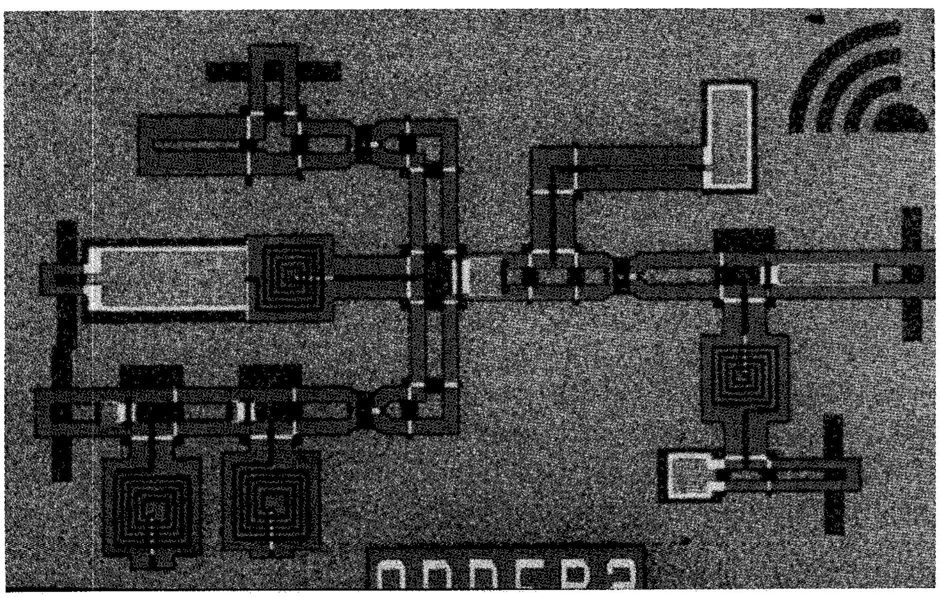

Fig. 1. Photo of a coplanar up-converter (*mixer4*)

INTRODUCTION

In the European research project ESPRIT CLASSIC mixers used as up- and down-converts between C- and V-band have been developed in microstrip (MS) and coplanar (CPW) technology utilising different strategies like diode- and FET-mixers, single-gate, dual-gate and cold-mixers etc. [2,3]. The field of applications for this efforts are the mobile communication systems such as MBS [1]. The coplanar MMICs have been fabricated at the Thomson TCS and Daimler Benz foundries in Paris and Ulm on GaAs utilising a pseudomorphic HEMT technology with a gate length of 0.15 μm and a gate witdth of 2 x 30 μm. The circuits have been developed with the harmonic balance simulators of MDS and Libra. Due to the lack of accurate HEMT models an improved Tajima model has been developed by IRCOM [5] and integrated into both simulators. With regard to mixer applications special care has been taken for pinch-off and cold biasing.

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MIXER DESIGN

This paper concentrates on the design of a coplanar up-converter from 5.2-7.2 GHz to 62-64 GHz. Four mixers with slight differences in the matching and the bias networks have been developed in total. Table 1 gives an overview of the properties of the mixers.

	size [mm^2]	$f_{converted}$ [GHz]	P_{LO} [dBm]	G_{Cmax} [dB]
mixer1	3.2	62 .. 66	0	8.5
mixer2	3.8	62 .. 66	2	4.7
mixer3	4.3	62 .. 64	2.5	12.5
mixer4	2.1	62 .. 64	6.5	11.3

Tab. 1. Comparison of the four mixer configurations

Nevertheless, the focus lies on *mixer4*, which has the smallest size and a high conversion gain. The goals were, to achieve up-converters with a small and a large bandwidth and to test the simulation tool with simplified biasnetworks for faster circuit optimization. The basic idea for all mixers was the same. This is depicted in the block-diagram of figure 2. The advantages of this configuration are the high LO to IF isolation due to the signal combining input stage as well as a high conversion gain by the use of amplifiers and a single gate FET mixer. The main problem during the design of the mixer was to develop the matching network, which minimises the attenuation of the strongly different input signals (LO: f_{LO}=56.8 GHz, 6.5 dBm; IF: -30 dBm) at the gate of the mixing device. This problem is increased by the need of reliable bias networks for the combiner and the mixer. To overcome these difficulties, accurate models for the coplanar elements as well as a stable and fast harmonic balance simulator must be available. The choice was Libra with the integrated coplanar library described in [4] and the modified Tajima model for the 2 x 30 μm HEMT with T-gates.

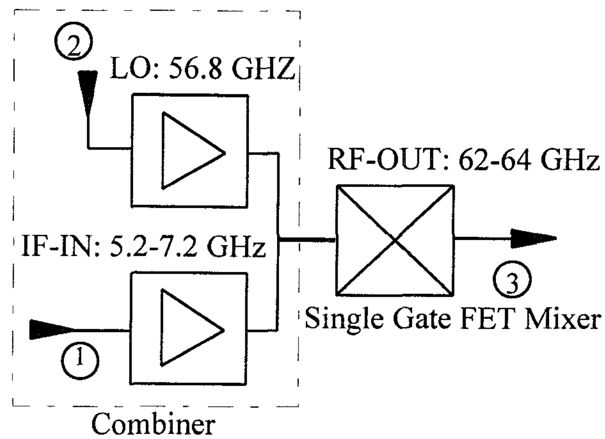

Fig. 2. Block-diagram of a CPW mixer

A photo of one of the fabricated circuits (*mixer4*) is illustrated in figure 1. The IF matching network was build up with lumped elements (MIMs and spiral inductors) while it is sufficient to use line stubs for the LO matching. An other big advantage of the coplanar technology becomes evident, if the block capacitors of the bias networks are considered. In contrast to the microstrip technology no parasitic via holes are necessary which are often inaccurately modelled and cause additional resonances. Moreover, the ground areas between the neighboured parts of the circuits prevent undesired coupling. All these advantages lead to a total circuit size of only 2.1 mm^2. A small-signal optimisation has been performed to achieve the best matching for the input signals and a stability criterion for the mixer. Since the LO is injected with 6.5 dBm, a large signal analysis and optimisation has to follow the S-parameter simulation to obtain the best conversion gain. This may reduce the small signal matching or lead to an undetected oscillation in the circuit, because nowadays it is not possible to combine small- and large-signal optimisation. The designer has to switch between both methods to achieve step by step the best performance. In the case of these mixer designs, the priority was a maximum conversion gain, which is larger than 4 dB in the desired frequency range.

EXPERIMENTAL RESULTS

Non-linear measurements have been performed by the IST in Lisbon, while the authors of the IMST have performed the simulation and the design of the circuit. The excellent agreement between the simulated and measured up-converter data depicted in figure 3 proves the validity of the coplanar models, the transistor model, the accurate power measurements and the repeatability of all technology. The experimental results of the four frequency converters is shown in figure 4. At the first sight, the conversion curves behave very similar. But, if we remember the specified bandwidth in table 1, one can see the high gain of *mixer3* and *mixer4* in the frequency range from 5.2 to 6.2 GHz. In opposite the conversion gain of *mixer1* and *mixer2* is more flat and greater than 0 dB nearly for all desired frequencies.

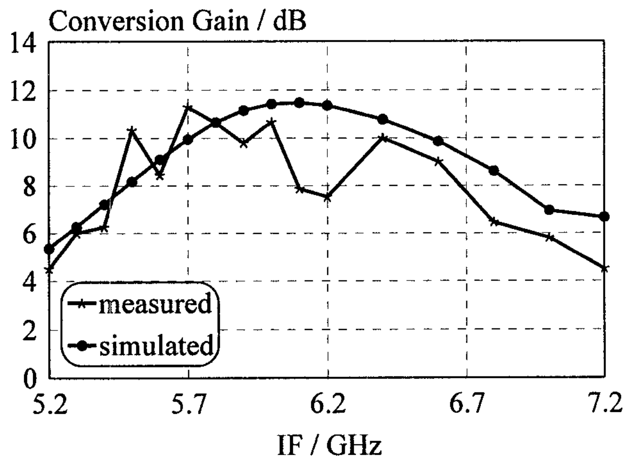

Fig. 3. Conversion gain of the coplanar upconverter *mixer4* (f_{LO} = 56.8 GHz)

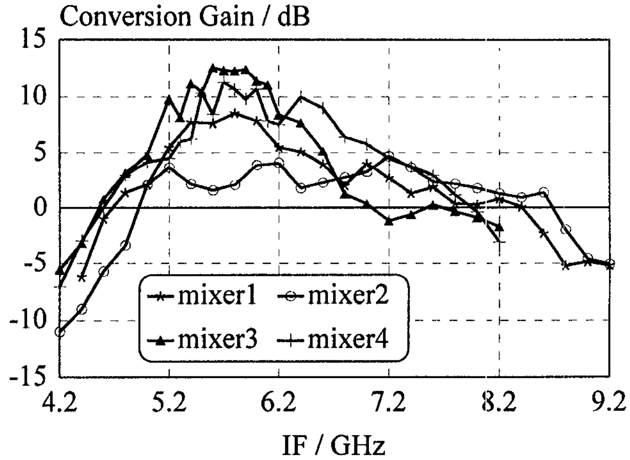

Fig. 4. Measured conversion gain of the four different coplanar upconverters

The linear measurements have been performed by the IMST. Since a small-signal three-port equipment up to 64 GHz was not available in the CLASSIC consortium, two-port measurements have been made by connecting a 50 Ω termination to the LO-input port. The simulated and experimental results of the S-parameters between port 1 and 3 (see figure 1) are illustrated by figures 5 and 6. $|S_{11}|$ in figure 5 shows the input matching of the IF. There is a good agreement between the theoretical and measured values up to 45 GHz. Beyond that frequency the inaccuracy of the model for the large spiral inductors (4.5 tracks) becomes evident, but does not influence the circuit behaviour. Figure 6 depicts the amplification of the IF signal (gain > 15dB). The isolation $|S_{13}|$ from the RF to the IF port is always lower than -30 dB, while the small signal matching of the RF port is about -8 dB. Although, as mentioned above, the small signal behaviour was neglected in the optimisation procedure. Therefore, the S-parameters should not be used for the interpretation of the mixers quality.

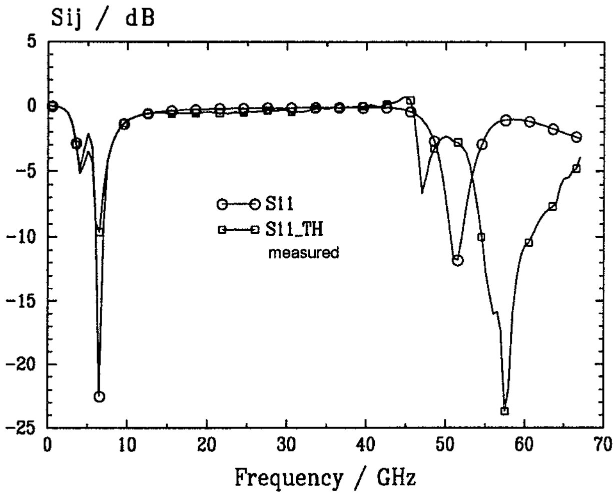

Fig. 5. Small signal return loss of IF (*mixer4*)

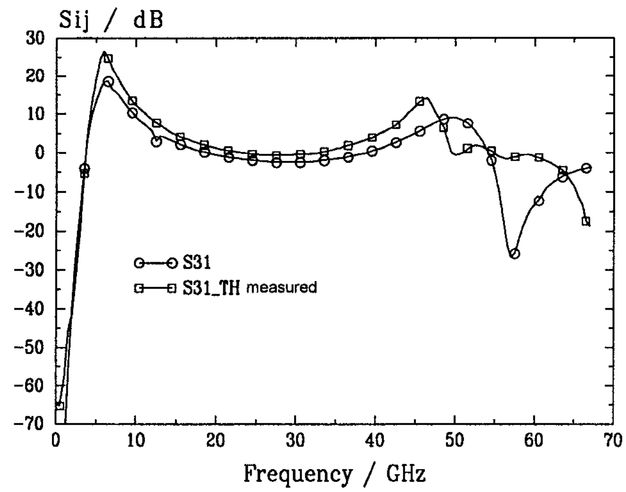

Fig. 6 Small signal amplification of IF signal (*mixer4*)

CONCLUSIONS

The design and evaluation of high gain up-converters from C- to V-band have been presented. These mixers have been fabricated in coplanar line technology on GaAs utilising PM-HFETs with a gate length of 0.15µm. Finally, a circuit size of only 2.1 mm^2 has been achieved. The conversion gain reaches more than 11 dB beyond 61 GHz. These results were possible with an accurate library for the modelling of the coplanar elements as well as the improved Tajima model for the non-linear simulation part.

ACKNOLEDGEMENTS

The work reported on in this paper was supported by the ESPRIT-CLASSIC projects. The authors would like to thank the responsible people at Daimler Benz and Thomson TCS for making the technologies available and for various discussions on technological details. We also would like to thank the partners of IRCOM (Limoge, France) for developing the non-linear models and supporting our designs with the extracted parameters for the HEMT models.

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